Wafer-Level Electrical Evaluation of Vertical Carbon Nanotube Bundles as a Function of Growth Temperature

Bart Vereecke1, Marleen H. van der Veen1, Masahito Sugira2, Yusaku Kashiwagi2, Xiaoxing Ke3, Daire J. Cott1, Thomas Hantschel1, Cedric Huyghebaert1, and Zsolt Tókei1

1 imec, Kapeldreef 75, Leuven, B-3001, Belgium
2 Tokyo Electron Ltd., Technology Development, Tsukuba, Ibaraki 305-0841, Japan
3 EMAT, University of Antwerp, Groenenborgerlaan 171, B-2020 Antwerp, Belgium

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We have evaluated the resistance of carbon nanotubes (CNTs) grown at a CMOS-compatible temperature using a realistic integration scheme. The structural analysis of the CNTs by transmission electron microscopy (TEM) showed that the degree of graphitization decreased significantly when the growth temperature was decreased from 540 to 400 °C. The CNTs were integrated to form 150-nm-diameter vertical interconnects between a TiN layer and Cu metal trenches on 200 nm full wafers. Wafers with CNTs grown at low temperature were found to have a lower single-contact resistance than those produced at high temperatures. Thickness measurements showed that the low contact resistance is a result of small contact height. This height dependence is masking the impact of CNT graphitization quality on resistance. When benchmarking our results with data from the literature, a relationship between resistivity and growth temperature cannot be found for CNT-based vertical interconnects.

1. Introduction

Carbon nanotubes (CNTs) are widely studied as an alternative to Cu interconnects because of their exceptional electrical1,2 and thermal3 properties. CNT can provide a low-resistivity vertical interconnect with a high aspect ratio that can sustain current densities4,5 up to 10⁹ A/cm², which is much higher than the Cu electromigration limit. In particular, the possibility to achieve ballistic charge transport6–8 is of great interest for future interconnect technologies.9) It allows for an increased aspect ratio of vertical interconnects without increasing resistance.

The objective of our work is to study the feasibility of using CNT interconnects in a CMOS integration scheme. However, the CNT growth and integration challenges for integration of CNTs remain significant10–16) In this paper we study the electrical resistance of CNT-based vertical interconnects of 150 nm diameter and grown at temperatures ranging from 400 to 540 °C. All processing was carried out at 200 nm wafer level in a CMOS fab and at growth temperatures down to CMOS-compatible temperatures.

2. Process for CNT Integration in 150 nm Contacts

The CNT contacts (Fig. 1) were fabricated on 200 nm Si wafers with TiN as the conducting bottom layer.17) On TiN, 50 nm Si₃N₄ was deposited followed by 360 nm phosphosilicate glass (PSG) and 30 nm SiC. The 150-nm-diameter holes were then dry etched followed by 60 s of 0.5% HF wet etch to create an undercut. Ar sputter cleaning of the TiN was applied prior to Ni catalyst placement by physical vapor deposition (PVD). The on-field thickness of Ni was targeted at 3 nm in order to reach ~1 nm at the bottom. Sidewall deposition was minimized by the HF undercut while the top SiC ensured selective CNT growth.18) Growth was carried out in a remote plasma chemical vapor deposition9) (CVD) reactor at wafer temperatures ranging from 400 to 540 °C. CNTs were grown after a catalyst pretreatment of 12 s in H₂ atmosphere at the growth temperature before introducing the carbon feed gas of the C₂H₂/H₂/Ar mixture at 40/45/1000 sccm and 3 Torr. The CNTs were encapsulated by atomic layer deposition (ALD) of 15 nm Al₂O₃ and sub-atmospheric CVD (SACVD) of a 60 nm SiO₂ layer17) to provide mechanical strength to the CNTs during the subsequent chemical–mechanical polishing (CMP). The Al₂O₃ ALD process was carried out using H₂O as the oxidant at 150 °C to achieve a mild process for the CNTs and provide good conformal filling.20) This CMP was used to remove excessive CNT material sticking out of the contact hole, to planarize the stack, and to open the tips of the CNTs. It is believed that opening the CNT tips could expose the inner shells to allow for better electrical contact with the top metal.21) The process continued with the deposition of the metallodielectric stack followed by metal trench patterning. The trench was filled by 15/10 nm TaN/Ta barrier deposition, followed by Cu plating and Cu CMP. Finally, the wafers were covered with a 4 nm SiC passivation layer.

3. Morphological Characterization

Figure 1 shows a transmission electron microscopy (TEM) cross-sectional view of a CNT-filled contact between the TiN bottom metal and the Cu metal trench with TaN/Ta barrier. Energy-filtered TEM was used for elemental analy-
sis. The carbon signals (green) show the CNT structures and the red dots correspond to the Ni signals. Ni is detected as particles at the bottom and on the sidewall of the contact hole. Because the Ni particles do not form a continuous film, we expect that there will be no parasitic conductive path through the Ni material on the sidewall of the contact hole. Hence, conduction must be through the inner area of the contact, that is, through the CNTs.

Scanning spreading resistance microscopy (SSRM) was performed on the contacts after the CMP step (Fig. 2). This technique uses an electrically conductive diamond probe for scanning the surface and simultaneously measuring the resistance underneath the probe tip. The SSRM zoom-in image in Fig. 2 shows small brown circular areas, which represent the electrical conductive CNTs inside the contacts. Note that the SSRM color contrast is set such that the non-conductive areas appear white and that the conductive areas appear as dark regions. This dotted pattern in each contact confirms that the main conduction mechanism is through the CNTs only, with no parasitic conduction paths via the sidewalls. In each contact hole, we find approximately 30 circular conductive areas corresponding to the individual CNT tubes. In a previous work, using 300-nm-diameter contact holes with a somewhat lower CNT density, it was found that the conducting areas form a continuous channel down to the bottom contact.

In order to investigate the structural quality and graphitization of the CNTs grown at different temperatures, we performed growth at 400, 440, and 540 °C on blanket TiN films using 1 nm Ni as a catalyst. Samples were analyzed by high-resolution TEM (Fig. 3) to study the graphitization of CNTs. The 540 °C sample showed well-aligned parallel CNT shells, while at lower temperature a clear degradation of the quality is observed. This results in the formation of bamboo-like structures for growth at 440 and 400 °C.

A similar TEM image [Fig. 3(d)] was obtained after full integration for the CNTs grown at 540 °C with Al2O3 encapsulation and after full integration. The image is less clear than that for the blanket samples as a result of the oxide encapsulation. However, the shell structure of the CNT is still visible and it shows that the integration process does not damage the CNT shells. It is expected that the morphological difference between samples grown at low and high temperatures will affect the electrical quality of the CNTs and, as such, will be reflected as a change in the resistance measurements.

4. Electrical Characterization of CNT Interconnects

The schematics in Fig. 4 show how single-contact-hole resistance ($R_{\text{single}}$) was measured by two techniques: four-
point probing of single contacts (Fig. 4, right) and two-point probing with a number of parallel contacts between each probing pad and the TiN bottom electrode. To improve the statistical accuracy for the resistance, we probed different structures with various numbers of vias \((N_1 \text{ and } N_2)\) in parallel. The formula

\[ R_{\text{meas}} = R_{\text{TiN}} + \frac{R_{\text{single}}}{N_{\text{par}}} \]

with \(\frac{1}{N_{\text{par}}} = \frac{1}{N_1} + \frac{1}{N_2}\) gives the measured resistance \(R_{\text{meas}}\) as a function of the number of vias in parallel \((N_{\text{par}})\). \(R_{\text{TiN}}\) is the resistance of the substrate and \(R_{\text{single}}\) is the resistance of a single 150 nm contact. The single-via resistance and the parasitic contribution from the TiN substrate can be extracted from the data by fitting. The slope is the resistance \(R_{\text{single}}\) of a single 150 nm contact, the interception at the \(1/N_{\text{par}} = 0\) is the contribution of the TiN substrate \((R_{\text{TiN}})\). As can be seen from Fig. 5, the \(R_{\text{TiN}}\) values obtained were similar for the three different wafers. Using a longer CMP time (50 s instead of 30 s) resulted in a lower resistance \(R_{\text{single}}\) (slope), and a smaller aspect ratio as can be seen from the scanning electron microscopy (SEM) images in the inset.

The resistance \(R_{\text{single}}\) for a single contact filled with CNTs can be split into three main contributors\(^{25} \) consisting of the top interface resistance \((R_1)\) at the CNT to the TaN top metal interface, the resistance \((R_2)\) resulting from the CNT itself, and the resistance \((R_3)\) from the bottom interface between the TiN and the CNT shells. A length analysis of CNT resistance could be used to separate the contact resistances\(^{26,27} \) \((R_1 + R_3)\) from the intrinsic CNT resistance \(R_2\). However, this method can only be valid if the density and number of connected tubes are identical for the samples of different lengths, which is difficult to achieve.

Ideally, the bottom plus top contact interface resistance consists of the quantum resistance of 6.5 kΩ per shell\(^{25} \) with no contribution from the ideal metallic CNTs that reach ballistic transport \((R_2 = 0)\) over sub-μm length. The ballistic transport property has been demonstrated and described in the literature for individual single-wall and multiwall CNTs.\(^{28} \) However, it proves challenging to integrate the CNTs at the wafer level using processes that are compatible with CMOS integration while maintaining the electrical properties that distinguish the CNTs from conventional metallic interconnects. To evaluate CNTs as an interconnect material, we integrated and evaluated the electrical performance of CNTs grown at CMOS-compatible temperatures.

The SEM analysis after the CNT growth (Fig. 6, top) confirms that CNT growth was achieved at all growth temperatures. The CNT growth time was set to 60 min for growth temperatures between 400 and 440 °C. The growth at 540 °C showed a significantly higher growth rate, and a shorter processing time of 10 min was used here. The bottom row in Fig. 6 shows images after oxide encapsulation and subsequent planarization by CMP. Overall, the number of CNTs extending from the via holes decreases with decreasing growth temperature, and the best filling was obtained for the growth at 540 °C.

We continued to evaluate the resistance of the contacts formed with CNTs produced at all temperatures (see also Fig. 3). The box plot (Fig. 7) shows the resistance measurements of CNT-filled contacts grown from 540 °C down to a CMOS-compatible temperature of 400 °C. For each wafer, 96 K structures were measured by four-point probing and the...
results were compared with measurements using the two-point probing technique reported elsewhere.\textsuperscript{17} A good agreement was found between the two methods. The parallel method yields slightly lower median values and gives a tighter distribution within the wafer, as is expected from the averaging effect when measuring contacts in parallel.

There is a clear trend towards a decreasing $R_{\text{single}}$ with decreasing growth temperature. This seems to be conflicting with the observations of a low density (Fig. 6, bottom) and low degree of graphitization (Fig. 3) for CNTs grown at low temperatures. A cross-sectional SEM analysis was carried out on all wafers to measure the length of the CNTs (i.e., height of the contacts) after full integration. It was found that the contact height for wafers grown at a low temperature is significantly smaller (Fig. 8). This phenomenon can be explained by the fact that the CMP removal behavior seems to correlate to growth temperature. The CMP process is influenced by 1) the length of the CNTs extending from the contact holes, 2) CNT density and the amount of carbon crust in the field area, and 3) the densification of the oxide when using high growth temperatures. As a consequence, contacts with CNTs grown at a low temperature (400°C) are overpolished compared to those grown at a higher temperature of 540°C. This contact height scaling is visualized in Fig. 9 where $R_{\text{single}}$ is plotted as a function of contact height. From this figure it is clear that despite the differences in the quality of graphitization, density, and growth temperature, the length is dominating the outcome of the resistance measurements. The fact that a length scaling is present suggests that the resistance of the CNTs is a major contribution and that the transport is far from being ballistic. Hence, much more work is needed to improve the integration of CNTs as vertical interconnects in order to reach ballistic behavior of the contact.

5. Comparison with the Literature

A large variety of techniques, process conditions, growth temperatures, and contact hole dimensions are used by different research groups to fabricate and evaluate vertical interconnects based on CNTs. In order to compare our results with data from the literature, we calculated resistivity and evaluated it as a function of the CNT growth temperature (Fig. 10). Note that resistivity is calculated from the total single-contact resistance and, hence, includes also the resistance contributions from the top and bottom contact interface. Despite the variety of processes, dimensions, and temperatures, most of the results are found in the same range as the results obtained in this work. Moreover, all the CNT resistivity values from integrated contact holes are more than two orders of magnitude above the resistivity value for Cu.\textsuperscript{29,30} CNT growth temperature is known to have an impact on CNT graphitization quality. However, no correlation between growth temperature and electrical resistivity is seen in Fig. 10.

6. Conclusions

We studied the resistance of CNT-filled contacts for CNTs produced at different growth temperatures. The electrical data were compared with morphological data on the CNT quality. It was found that the CNT graphitization improved when the growth temperature was increased from 400 to 540°C. However, this trend was not found from the electrical results. We found that contact resistance was dominated by length, thereby masking the impact of CNT quality. This suggests that improvement in the integration is needed in order to be able to probe CNT quality electrically. The contact resistivity obtained in this work is in the same range as other results reported in the literature. The benchmarking of the available resistivity data shows that the conduction mechanism for vertical integrated CNTs is far from the ideal ballistic transport, independently of
the growth temperature or integration process used. Our electrical evaluation shows that it remains challenging to achieve CNT interconnects using realistic integration schemes while preserving the electrical properties that distinguish CNTs from conventional metals.

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